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UNDER THE PATENT COOPERATION TREATY-CHAPTER II

APPLICANT: Peter Liggesmeyer DOCKET NO: P99,0101
SERIAL NO: GROUP ART UNIT:
EXAMINER:

INTERNATIONAL APPLICATION NO: PCT/DE98/00633
INTERNATIONAL FILING DATE: 03 MARCH 1998
INVENTION: **METHOD FOR COMPUTER-SUPPORTED ERROR ANALYSIS OF SENSORS AND/OR ACTUATORS IN A TECHNICAL SYSTEM**

Assistant Commissioner for Patents,
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT
According to 37 C.F.R. 1.97(b)

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and the requirements of 37 C.F.R. 1.98, Applicant respectfully requests that a citation and examination of the references identified on the attached PTO 1449 form be made during the course of examination of the above-identified application for United States Patent.

The present Information Disclosure Statement is being filed according to 37 C.F.R. 1.97(b) and before the latter occurrence of:

(1) three months from the filing date of a national application;

(2) three months from the date of entry of the national stage as set forth in 37 C.F.R. 1.491 in an international

application; or

(3) the mailing date of a first Office Action on the merits.

REMARKS

The attached PTO 1449 form lists prior art references identified in the International Search Report, copy of which is enclosed herewith.

European reference EP 0 424 869 A1 dated 02 May 1991;

European reference EP 0 352 759 B1 dated 31 January 1990, (corresponding to U.S. Patent 5,107,425 dated 21 April 1992);

European reference EP 0 580 663 B1 dated 02 February 1994, (corresponding to U.S. Patent 5,491,639 dated 13 February 1996);

European reference EP 0 685 792 A1 dated 06 December 1995, (corresponding to U.S. Patent 5,615,137 dated 25 March 1997);

Articles:

Burch, Jerry R. et al, "SYMBOLIC MODEL CHECKING FOR SEQUENTIAL CIRCUIT VERIFICATION", IEEE Transactions on Computer-Aided Design of Integrated Circuits and systems, Vol. 13, No. 4, April (1994), pp. 401-424; and

Enders, Reinhard et al, "GENERATING BDDS FOR SYMBOLIC MODEL CHECKING IN CCS", Computer Aided Verification 3rd, July (1991), pp. 203-213.

Articles cited in the specification:

DIN 25424, Part 1: Fehlerbaumanalyse: Methode und Bildzeichen; Part 2: Handrechenverfahren zur Auswertung eines Fehlerebaums;

Dekleer, J. et al, DIAGNOSING MULTIPLE FAULTS, Elsevier Science Publishers, Artificial Intelligence, Vol. 32, 1987, pp. 97-130;

Nökel, K. et al, CONTROLLER SYNTHESIS AND VERIFICATION: A CASE STUDY, in: C. Leverentz, T. Lindner, Formal Development of Reactive Systems, Lecture Notes in Computer Science (No. 891), Springer 1995, pp. 55-74; and

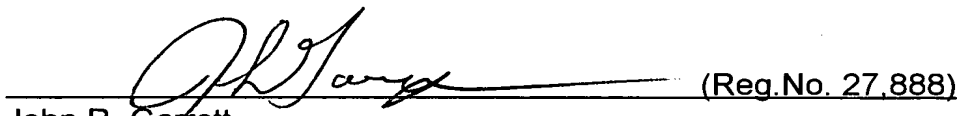
Bryant, R., SYMBOLIC BOOLEAN MANIPULATION WITH ORDERED BINARY-DECISION DIAGRAMS, ACM Computing surveys, Vol. 24, No. 3, September (1992), pp. 293-318.

The documents may have markings thereon, however, no significance is meant to be attached to the markings.

The filing of the present Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed as an admission that the information cited in the present Information Disclosure Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56(b).

The above citation of prior art is not a representation that such art constitutes a complete or exhaustive listing of all pertinent prior art, nor that it necessarily includes the closest or most relevant art. The aforementioned citation comprises a voluntary citation of prior art of which applicant and his attorney are presently aware and is not intended to serve as a substitute for the Examiner's own search.

Respectfully submitted,



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